**ABSTRACT**

A method of manufacturing chalcogenide memory in a semiconductor substrate. The method includes the steps of forming a N+ epitaxy layer on the semiconductor substrate; forming a N- epitaxy layer on the N+ epitaxy layer; forming a first STI in the N+ and N- epitaxy layers to isolate a predetermined word line region; forming a second STI in the N- epitaxy layer to isolate a predetermined P+ doped region; forming a dielectric layer on the N- epitaxy layer; patterning the dielectric layer to form a first opening and performing a N+ doping on the N- epitaxy layer via the first opening such that a N+ doped region is formed in the N- epitaxy layer and connected to the N+ epitaxy layer; patterning the dielectric layer to form a second opening and performing a P+ doping on the N- epitaxy layer such that a P+ doped region is formed; forming contact plugs in the first opening and the second opening respectively; and forming an electrode on each contact plug, wherein the electrode includes a lower electrode, a chalcogenide layer and an upper electrode.